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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,522	07/08/2003	Jeremy A. Theil	MICR-153US	9342

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EXAMINER	
SELBY, GEVELL V	
ART UNIT	PAPER NUMBER
2622	
MAIL DATE	DELIVERY MODE
07/15/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/615,522	THEIL ET AL.	
	Examiner	Art Unit	
	GEVELL SELBY	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5,6,8-18 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5,6,8-16 and 18* is/are rejected.

7)☒ Claim(s) *17 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1, 5, 6, 8-18, and 20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 5, 6, 8-16, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsunaga et al., US 2001/0013901.

In regard to claim 1, Matsunaga et al., US 2001/0013901, discloses an image sensor, comprising:

multiple pixels (see figure 31, elements P11-1-1 to P11-3-3) each including a respective photodiode region (see para 184);

pixel circuits (see figure 31, element 5, 13, and P11-i-j) each operable to control integration and readout steps for a respective pixel (see para 68-74); and

a bias circuit (see figure 31, elements 6-1 to 6-n) operable to apply voltages across the pixels to forward bias the photodiode regions during a reset step for each pixel (see para 18 and 190), wherein it is inherent the bias circuit of

the Matsunaga can be used in a charge blanking step for each pixel, since the structure to bias is disclosed.

In regard to claim 5, Matsunaga et al., US 2001/0013901, discloses the image sensor of claim 1, wherein pixels are arranged in an array of multiple rows and the bias circuit is operable to simultaneously induce forward bias flow of injected carriers through the photodiode regions of all pixels in a given row of the array (see para 190: all the pixels are reset simultaneously, so each row is reset simultaneously).

In regard to claim 6, Matsunaga et al., US 2001/0013901, discloses the image sensor of claim 5, wherein the bias circuit is operable to simultaneously induce forward bias flow of injected carriers through the photodiode regions one row at a time (see fig 32: the forward bias is injected one column at a time, which is equivalent to one row at a time, when the image sensor is rotated 90 degrees).

In regard to claim 8, Matsunaga et al., US 2001/0013901, discloses the image sensor of claim 5, wherein it is inherent the image sensor of the Matsunaga reference is operable or can be used to simultaneously induce forward bias flow of injected carriers through photodiode regions of all rows in the array, since the structure of the image sensor is disclosed.

In regard to claim 9, Matsunaga et al., US 2001/0013901, discloses the image sensor of claim 1, wherein it is inherent the bias circuit of the Matsunaga reference is operable or can be used to induce carrier injection between photodiode regions of pixels, since the structure of the bias circuit is disclosed.

In regard to claim 10, Matsunaga et al., US 2001/0013901, discloses the image sensor of claim 1, wherein it is inherent the bias circuit of the Matsunaga reference is operable or can be used to induce carrier injection between photodiode regions of adjacent pixels, since the structure of the bias circuit is disclosed.

In regard to claim 11, Matsunaga et al., US 2001/0013901, discloses the image sensor of claim 10, wherein the bias circuit is operable to apply different voltage levels to nodes of adjacent pixels (see figure 32: adjacent rows are reset with a different voltage than normal operation sequentially).

In regard to claim 12, Matsunaga et al., US 2001/0013901, discloses the image sensor of claim 11, wherein it is inherent the bias circuit of the Matsunaga reference is operable or can be used to apply different high-to-low voltage ranges across adjacent pixels, since the structure of the bias circuit is disclosed.

In regard to claim 13, Matsunaga et al., US 2001/0013901, discloses the image sensor of claim 11, wherein pixels are arranged in an array of multiple rows (see figure 31) and the bias circuit is operable to apply different voltage levels to nodes of adjacent pixels in adjacent rows (see figure 32: adjacent rows are reset with a different voltage than normal operation sequentially).

In regard to claim 14, Matsunaga et al., US 2001/0013901, discloses the image sensor of claim 11, wherein pixels are arranged in an array of rows and columns (see figure 31) and it is inherent the bias circuit of the Matsunaga reference is operable or can be used to apply different voltage levels to nodes adjacent pixels in adjacent rows and to

apply different voltage levels to nodes of adjacent pixels in adjacent columns, since the structure of the bias circuit is disclosed.

In regard to claim 15, Matsunaga et al., US 2001/0013901, discloses the image sensor of claim 10, wherein the different voltage levels applied to nodes of adjacent pixels are switched periodically (see figure 32).

In regard to claim 16, Matsunaga et al., US 2001/0013901, discloses the image sensor of claim 10, wherein the bias circuit includes two bias lines for applying different respective voltage levels to the pixels (see figure 31, element 6-1 and 6-2).

In regard to claim 18, since Matsunaga et al., US 2001/0013901, discloses the image sensor and its operation as described in regard to claim 1 above, the method of operating the sensor is also disclosed.

Allowable Subject Matter

4. Claims 17 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GEVELL SELBY whose telephone number is (571)272-7369. The examiner can normally be reached on 8:00 A.M. - 5:30 PM (every other Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on 571-272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

gvs

/Lin Ye/
Supervisory Patent Examiner, Art Unit 2622